Abstract—We propose a novel one-level simplification method for all-optical combinational logic circuits. With the proposed method, an all-optical gray code to binary coded decimal converter is successfully developed for the first time by using conventional semiconductor optical amplifiers as building elements. In comparison to the construction algorithm based on the conventional two-level simplification method, a significant improvement is observed in the $Q$-factor.

Index Terms—All-optical logic circuits, cross-gain modulation (XGM), semiconductor optical amplifier (SOA).

I. INTRODUCTION

Cross-gain modulation (XGM) in semiconductor optical amplifiers (SOAs) has attracted attention for a long time, particularly from researchers in the field of all-optical signal processing. Inferior to cross-phase modulation (XPM)-based SOA logic elements [1] with regard to their general performance (such as $Q$-factor, extinction ratio), but still with their simplicity in structure, advanced devices have been developed thus far for all-optical signal processing based on XGM dynamics in SOAs, for example, wavelength converters [2], [3], regenerators [4], [5], optical gates [5]–[9], and memory elements [10]. In a limited scope, higher level integrated devices such as combinational logic circuits [11] have also been demonstrated recently in the form of half-adders [12]. However, regarding the future realization of full-scale combinational (memory-less) logic circuits such as encoder/decoder, mux/demux, and read-only memories, several technical issues are yet to be resolved, for example, the development of multi-input-port all-optical gate structures and their application method for the simplification of high-level logic circuits, the establishment of systematic design rules for digital photonic circuits by taking into account the peculiarities/advantages of photonics, and the mitigation of signal quality degradation at the circuit design level.

A partial solution for the abovementioned problems has recently been suggested [13] by employing an XGM-based SOA NOR gate that accepts multiple input signals, and directly applying the two-level simplification method (widely adopted in digital electronics). However, due to the inherent limitation, namely, the accumulation of a patterning effect from SOA cascades, the resulting signal quality was still too poor.

In this letter, as an extension of our previous work [13], we propose a novel one-level simplification design method (1LSM) so termed to differentiate it from the conventional two-level simplification method (2LSM) used in digital electronics [11]; keeping consistency of the terminology of level with that of digital electronics, not counting NOT-gate as one of the level) in order to minimize the accumulation of signal degradation and to provide a systematic construction method for higher level combinational photonic logic circuits. By using a multi-input NOR gate as employed in [13] to achieve a minimal usage of the required logic elements, and by subsequently using the newly proposed photonic specific all-optical 1LSM, we numerically demonstrate the successful operation of a 4-bit gray code (binary numeral system where two successive values differ by only one digit) to a 4-bit binary coded decimal (BCD) converter, for the first time, to our knowledge. Compared to the circuit based on the 2LSM, a significant improvement in the $Q$-factor was observed with the 1LSM-based converter.

II. THEORY

The XGM-based SOA NOR gate is used as the basic building block for the construction of all-optical combinational logic circuits—taking its advantages such as 1) polarization insensitivity and structural simplicity (as compared to other logic gates; it should be noted that a NOR gate can be constructed using a single SOA [14], whereas two SOAs are required for the construction of AND [6], OR [7], XOR [8], or NAND gates [15]); and 2) higher performance factors (better $Q$ with only one SOA used in the device). It should also be noted that an SOA NOR gate has a unique capability of accepting multiple input signals, thereby enabling the construction of higher level circuits with simpler structures as compared to circuits employing other types of logic elements (Fig. 1). It is also worth mentioning that care must be taken in the design of the circuit to avoid interference of the signal from same sources: e.g., using incoherent signal source, adjusting length of arms, or taking counterpropagating (or color) signal source.

Assuming a NOR gate as the basic building block, now in order to reduce the number of logic gate cascades (and thus to suppress the accumulation of signal quality degradation), the conventional 2LSM was modified to best correspond to the properties of optical logic circuits. Fig. 2 shows the examples of a NOR–NOR 2LSM optical circuit and NOR 1LSM circuit for the Boolean operation $F = (A + B)\bar{C}$, illustrated/tested for the proof of principle (construction algorithm detailed later).

To note, in the 1LSM, the NOR gate cascade in the conventional 2LSM structure is replaced with the one-level optical NOR gate structure to avoid the ER penalty accumulation in SOA cascades. From the figure of the 1LSM circuit with a reduced number of NOR cascades, it can be observed that it is possible to...
Fig. 1. Illustration of all-optical logic gates with multiple inputs ($m = 3$).

Fig. 2. Comparison of (a) conventional 2LSM and (b) proposed 1LSM structures and their performances. RZ signals were assumed to be 2.5 Gb/s.

obtain a better eye (extinction) for the final data (for this circuit, $Q$-factors of 3.8 and 5 are obtained by the 2LSM and 1LSM approaches, respectively).

It is important to note that, for the practical implementation of the 1LSM for combinational optical logic circuits, the general procedure (with the example in Fig. 2) is as follows: A) draw a Karnaugh map for the given operation/truth table, B) follow the conventional AND–OR 2LSM procedure to draw a digital circuit while avoiding the symbol selection overlaps (i.e., avoid “1” OR “1” in the Karnaugh map) [11], [16], and C) substitute the OR gates with optical power sums. Further, convert the AND gates to NOR by utilizing DeMorgan’s theorem [11].

It is noteworthy that by removing the selection overlaps in step B, it is possible to prevent two or more input symbols “1” from entering the OR gate; this implies that under this arrangement, the OR gates can be safely replaced by simple optical power sums. Thus, with fewer nonideal optical elements (in this case OR gate) in the circuit, signal degradation can be efficiently reduced.

Fig. 3. Schematic of all-optical gray code to BCD converter constructed using the 2LSM (left) and the proposed 1LSM (right).

III. RESULTS

As an application of the proposed method, a gray code to BCD converter was constructed by following the procedure described in Section II. Fig. 3 shows the schematic of the all-optical gray code to BCD converter constructed with the proposed 1LSM and conventional 2LSM approaches for comparison purposes. Each bit of the 4-bit gray code is labeled from $A$ to $D$ starting from the most significant bit (MSB) to the least significant bit (LSB). The output signals of the BCD, labeled from $W$ to $Z$, are extracted from the corresponding ports of the converter. For the 1LSM-based circuit, as many as 12 SOAs (14 SOAs for 2LSM) were required to complete all the Boolean operations shown in the truth table [Fig. 4(a)].

It should be noted that for any type of combinational logic circuit, the maximum number of SOA gate cascades required in the 1LSM and 2LSM structures are two and three, respectively. Not critical but also worth mentioning, attenuators/erbium-doped fiber amplifiers are assumed (not shown in Fig. 3) to optimize the power levels of the propagating signals for an efficient XGM process, which is in general dependent on the signal power level, pulse shape, and SOA injection current [5].

Fig. 4 shows the output data traces of the gray code to BCD converter output with 2.5-Gb/s input signals (sequentially starting from decimal numbers “0” to “9” in gray code expression, taking numbers between “10” and “15” under the “don’t care condition”). $2^7 - 1$ pseudorandom bit sequence (PRBS) patterns to the input ports of the converter (with different PRBS seed values) were also tested to obtain the eye diagrams at each output port in order to study the device performance for random input sequences of gray codes. It is noteworthy that the return-to-zero (RZ) signal format was used instead of the nonreturn-to-zero signal format to avoid the static “1” hazard due to the finite rising/falling time [11].

Evidently, severe degradation can be observed from the data in the case of the 2LSM approach. In contrast, using the proposed 1LSM approach, a clear eye opening is obtained, thereby providing a reliable conversion between the two codes. For this specific device and SOA parameter setting (Table I), the measured $Q$-factors were 7, 7, and 4 for each output of $X$, $Y$, and $Z$. 
The $Q$-factor obtained by the proposed 1LSM approach is significantly better than that obtained by the 2LSM approach (1.5 ≈ 4: from 7, 2.8, and 2.4 with 2LSM to 7, 7, and 4 with 1LSM for symbols $X$, $Y$, and $Z$, respectively). It should be noted that it is possible to apply our 1LSM approach to the all-optical logic gate based on the XPM dynamics of SOA for even better performances at the expense of increased device complexity. We believe that the proposed 1LSM approach would aid in the systematic design of high-performance, high-complexity combinational all-optical photonic circuits, thereby complementing the unexplored area of digital photonic circuit theories.

REFERENCES