All-optical 4-bit Gray code to binary coded decimal converter

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ABSTRACT

All-optical 4-bit *Gray* code to *binary coded decimal* (BCD) converter was demonstrated, for the first time in our knowledge, with the number of 12 SOAs by means of commercially available numerical analysis tool (VPI). Circuit design approach was modified appropriately in order to fit the electrical method on an all-optical logic circuit based on cross gain modulation (XGM) process so that signal degradation due to the non-ideal optical logic gates can be minimized. In our approach, only using XGM process as a nonlinear function, the maximum number of XGM process serially underwent by input signals is twice at the most insuring signal quality. Without regenerations, Q-factor of around 4 was obtained for the most severely degraded output bit (least significant bit - LSB) with 2.5Gbps clean input signals having 20dB extinction ratio. It is worth to note that, implementing this LSB is complex enough to give it as an example of a 4-bit conversion system. While modifying two-level simplification method and *Karnaugh* map method to design *Gray* code to BCD converter, general design concept was also founded in this research not only for the *Gray* code to BCD converter but also for any general applications such as encoder / decoder, multiplexer / demultiplexer, and read only memory so that readers can develop their own all-optical logic device easily using XGM process in SOAs.

Keywords: all optical converter, binary coded decimal, combinational logic circuit, cross gain modulation, gray code, one level simplification method, semiconductor optical amplifier, two level simplification method

1. INTRODUCTION

All optical signal processing has attracted attention for a long time and various all optical *Boolean* logic gates has been implemented [1, 2, 3, 4, 5, 6] by means of cross phase modulation (XPM; employing Nonlinear Optical Loop Mirror [7], Terahertz Optical Asymmetric Demultiplexer [8], *Mach-Zehnder* Interferometer, Ultrafast Nonlinear Interferometer [9]) cross gain modulation (XGM), four wave mixing and Kerr effect at high-Q cavity. Even though there are some demonstrated combinational (memory-less) logic circuit such as adder and subtractor [10, 11, 12], more complex all optical combinational logic circuit has not been reported yet. Because, it is still hard to implement complex combinational logic circuit all-optically by the reasons of many problems which are arose due to large system scale and non-ideal all optical logic gate elements. For example, accumulations of noise and extinction ratio degradation can prevent implementation of complex all optical combinational logic circuits. Thus, study on implementation of more complex all optical combinational logic circuits such as coder / decoder should be done. All-optical *Gray* code to *binary coded decimal* (BCD) which has not been demonstrated yet seems complex enough to study for this issues as a kinds of coder / decoder system (BCD to *Gray* code is much easier to implement). BCD is an encoding for decimal numbers in which each digit is represented by its own binary sequence and *Gray* code is another binary numeral system where two successive values differ in only one digit.

In this paper, first of all, studies are carried out about implementation of an all-optical 4-bit *Gray* code to BCD converter directly employing digital electronic method termed as NOR-NOR two-level simplification method. It should be noted that whole demonstrations in this paper are made by logic gates based on XGM process. This is because its simplicity makes circuit implementation much easier though its performance is worse than that of the case based on XPM when it comes to operation speed and extinction ratio. It is possible to construct circuit utilizing only XGM process because all of the *Boolean* logic gates can be implemented all-optically by means of XGM in semiconductor optical amplifiers (SOAs). Secondly, one-level simplification method is proposed which is well-fitted on the optical circuit. Third, we implement an all-optical 4-bit *Gray* code to BCD converter utilizing above proposed one-level simplification method. Fourth, comparisons between two-level simplification method and one-level simplification method are provided with results and additional issues associated with one-level simplification method are discussed.

2. DESIGN WITH TWO-LEVEL SIMPLIFICATION METHOD

The design procedure of *Gray* code to BCD converter with two-level simplification using electronic components is well known in the fields of digital electronics and also it is described well in many electronic textbooks [13]. To design gray code to BCD converter with optical components brief illustration of a part of well known design procedures developed for electronics are presented especially which can be used for the optical design. And then details are explored about design considerations arisen by using optical components.

2.1 Digital electronic theory for all-optical *Gray* code to BCD converter

In our design, NOR-NOR two-level simplification method will be chosen due to its simplicity of optical structure and ability of accepting multiple input ports as will be described later. To do this, first of all, *Karnaugh* map [14] was drawn as it is shown in the Fig. 1 with the truth table shown in the Table 1. Above the decimal number of '9' was designated as '*Don't care condition*' which means that user don't care whether the output value of the system becomes 1-level or 0-level [13]. And, each bit of the 4-bit *Gray* code is labeled as "A" to "D" starting from the MSB (most significant bit) to the LSB (least significant bit) and each bit of the BCD is labeled as "W" to "Z" starting from the MSB to the LSB.

Table 1. Truth table for the *Gray* code to BCD converter

Decimal	Gray Code				BCD			
	A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	1	0	0	1	0
3	0	0	1	0	0	0	1	1
4	0	1	1	0	0	1	0	0
5	0	1	1	1	0	1	0	1
6	0	1	0	1	0	1	1	0
7	0	1	0	0	0	1	1	1
8	1	1	0	0	1	0	0	0
9	1	1	0	1	1	0	0	1
10	X	X	X	X	X	X	X	X
11	X	X	X	X	X	X	X	X
12	X	X	X	X	X	X	X	X
13	X	X	X	X	X	X	X	X
14	X	X	X	X	X	X	X	X
15	X	X	X	X	X	X	X	X

Fig. 1. *Karnaugh* map for the NOR-NOR two-level simplification method to design *Gray* code to BCD converter

From the above drawn *Karnaugh* map two-level simplified *Boolean* equation was obtained as *product of sums* (AND of OR) form for the each output as the Eq. 1.

$$W = A \quad (1a)$$

$$X = \overline{A}B \quad (1b)$$

$$Y = \overline{A}(B+C)(\overline{B}+\overline{C}) \quad (1c)$$

$$Z = (B+C+D)(\overline{A}+C+D)(A+\overline{B}+C+\overline{D})(B+\overline{C}+\overline{D})(\overline{B}+\overline{C}+D) \quad (1d)$$

Then, NOR-NOR two-level simplified *Boolean* equation can be obtained as the Eq. 2 by utilizing DeMorgan's theorem [13] from the Eq. 1.

$$W = A \quad (2a)$$

$$X = \overline{\overline{A+B}} \quad (2b)$$

$$Y = \overline{\overline{A + (\overline{B+C}) + (\overline{B+C})}} \quad (2c)$$

$$Z = \overline{\overline{(B+C+D) + (\overline{A}+C+D) + (A+\overline{B}+C+\overline{D}) + (B+\overline{C}+\overline{D}) + (\overline{B}+\overline{C}+D)}} \quad (2d)$$

From the Eq. 2 schematic circuit was obtained with NOT and NOR gates as in the Fig. 2.

Fig. 2. Schematic diagram of designed *Gray* code to BCD converter utilizing the NOR-NOR two-level simplification method.

2.2 All-optical implementation

In order to implement this circuit with optical components, all-optical NOT and NOR gates are required. As we know the NOT gate has the simplest structure thus we did not show its structure. And, other type of all-optical logic gates that accept three input port were constructed in the Fig. 3 (a) to show their complexity. As we mentioned earlier NOR-gates have the simplest structure in general while it is accepting multiple input-port as you can see in the Fig. 3 (a). Also it should be noted that a NOR gate can be constructed using a single SOA [6] for multiple input ports whereas two SOAs are required for the construction of AND [1], OR [3], XOR [4], or NAND gates [5] even for two input ports. That is the reason why NOR-NOR two-level simplification is the most suitable for all-optical implementation among various method (There are other ways to construct combinational logic circuits such as AND-OR or OR-NOR or NAND-NAND two-level simplification method [13]). The above designed structure for the all-optical *Gray* code to BCD converter was constructed all optically as Fig. 3 (b) directly using all optical NOR gates shown in the Fig. 3 (a) as the basic building block.

Fig. 3. (a) Structures of various all-optical logic gates accepting three input ports utilizing XGM in SOAs. (b) Designed Structure for all-optical *Gray* code to BCD converter utilizing NOR-NOR two-level simplification method

3. PROPOSAL OF ONE-LEVEL SIMPLIFICATION METHOD

Here the one-level simplification method which is more suitable to the all-optical circuit is proposed. Details are described with an example for arbitrary functional system in which output is obtained corresponding to the input combination of signal A, B, and C as shown in Table 2 (*Boolean* operation of $F = (A + B)\overline{C}$).

Table 2. Truth table for arbitrary functional system that will be used to illustrate one-level simplification method as an example

Input	A	0	0	0	0	1	1	1	1
	B	0	0	1	1	0	0	1	1
	C	0	1	0	1	0	1	0	1
Output	F	0	0	0	0	1	1	1	0

When this arbitrary example (*Boolean* operation of $F = (A + B)\overline{C}$) is designed utilizing conventional NOR-NOR two-level simplification method, procedure is same as above described *Gray* code to BCD converter. And its implementation was shown in the Fig. 4 (a) with an eye diagram result for given SOA parameters set of Table 3. After optimization of XGM process in SOAs the Q factor of around 3.8 was observed with the 20dB extinction ratio input RZ signal at 2.5Gbps (To focusing on the theory of one-level simplification method, detail optimization process is skipped and will be presented in the next chapter).

Now in order to reduce the number of logic gate cascades (so that accumulation of signal quality degradation can be suppressed), the conventional two-level simplification was modified as one-level to best corresponds to the properties of all-optical logic circuits. The Fig. 4 (b) shows implementation of the system with the one-level simplification method and an eye diagram result shows Q factor improvement resulting in the value of around 5. Design procedure is summarized as follow:

- (A) Draw a Karnaugh map for the given operation/truth table.
- (B) Follow the conventional AND-OR two-level simplification procedure to draw a digital circuit while avoiding the symbol selection overlaps (i.e., avoid “1” OR “1” in the Karnaugh map) [14].
- (C) Substitute the OR gates with optical power sums. Further, convert the AND gates to NOR by utilizing DeMorgan’s theorem [13].

In step (B), it should be noted that two or more input symbols “1” entering the OR gates at the same time can be prevented by removing the selection overlaps. The OR gates thereby can be safely replaced by simple optical power sums. Then, signal degradation can be efficiently reduced by removing non-ideal optical element level in the circuit while make it simple to implement.

Table 3. SOA Parameters for numerical simulation

Name	Value	Name	value
Driving current	200 mA	Transparent carrier density	$1.5 \times 10^{24} \text{ m}^{-3}$
Active region length	350 μm	Material gain coefficient	$3 \times 10^{-20} \text{ m}^2$
Active region width	2.5 μm	Internal loss	$3,000 \text{ m}^{-1}$
Active region thickness	0.04 μm	Group effective index	3.7
ASE spectral width	1 THz	Facet reflectivity	0.0001

Fig. 4. Comparison of (a) conventional two-level simplification method and (b) proposed one-level simplification method structures and their performances. RZ signals were assumed to be 2.5 Gbps.

As you can see in the Fig. 4, in the one-level simplification method, the NOR gate cascade in the structure of conventional two-level simplification method is replaced with just NOR gate structure avoiding the ER penalty accumulation in SOA cascades. It can be observed from the designed optical circuit that it is possible to construct same system with the reduced number of NOR cascades with a better eye (and also better extinction) for the final data. It should be noted that for any type of combinational logic circuit, the maximum number of XGM cascades required in the one-level simplification method and two-level simplification method are two and three, respectively. It is also worth to mention that any general applications such as encoder / decoder, multiplexer / demultiplexer, and read only memory are suitable to this proposed one-level simplification method.

4. DESIGN WITH ONE-LEVEL SIMPLIFICATION METHOD

Following above mentioned step (A) and (B), first of all, *Karnaugh* map [14] was drawn as it is shown in the Fig. 5 with the truth table shown in the Table 1. And symbols were selected carefully without overlap differently against the conventional two-level simplification method.

Fig. 5. *Karnaugh* map for the one-level simplification method to design *Gray* code to BCD converter

From the above drawn *Karnaugh* map two-level simplified *Boolean* equation was obtained as *sum of products* (OR of AND) for the each output as the Eq. 3.

$$W = A \quad (3a)$$

$$X = \overline{AB} \quad (3b)$$

$$Y = \overline{ABC} + \overline{BC} \quad (3c)$$

$$Z = \overline{ABCD} + \overline{ABCD} + BCD + \overline{ACD} + \overline{BCD} \quad (3d)$$

Then, following step (C), the OR gate was converted as the optical power sum and this yield following Eq. 4.

$$W = A \quad (4a)$$

$$X = \overline{A + B} \quad (4b)$$

$$Y = (\overline{ABC})sum(\overline{BC}) \quad (4c)$$

$$Z = (\overline{ABCD})sum(\overline{ABCD})sum(BCD)sum(\overline{ACD})sum(\overline{BCD}) \quad (4d)$$

Further, AND operation in Eq. 4 was converted as NOR operation by utilizing DeMorgan's theorem [13] as the Eq. 5.

$$W = A \quad (5a)$$

$$X = (A + \overline{B}) \quad (5b)$$

$$Y = (\overline{A + \overline{B} + C}) \text{sum}(\overline{B + \overline{C}}) \quad (5c)$$

$$Z = (\overline{A + \overline{B} + C + D}) \text{sum}(\overline{A + B + C + \overline{D}}) \text{sum}(\overline{\overline{B} + \overline{C} + \overline{D}}) \text{sum}(\overline{\overline{A} + C + \overline{D}}) \text{sum}(\overline{B + \overline{C} + D}) \quad (5d)$$

From the Eq. 5 schematic diagram and all-optical circuit were designed as shown in the Fig. 6. Compared to the converter with two-level simplification method which requires number of 14 SOAs, designed converter here with one-level simplification method requires number of 12 SOAs to complete the same *Boolean* function. Also note that, as mentioned in the earlier chapter, the maximum number of XGM cascades is only two.

(a) Schematic diagram of designed Gray code to BCD converter utilizing the one-level simplification method

(b) Designed all-optical Gray code to BCD converter with the one-level simplification method

Fig. 6. Design results of *Gray* code to BCD converter with one-level simplification method

5. RESULTS

The XGM process should be optimized to evaluate designed all-optical Gray code to BCD converter. Attenuators and EDFAs were used even it was not shown in Fig. 3 and Fig. 6 to optimize the power levels of the propagating signals for an efficient XGM process, which is in general dependent on the signal power level, pulse shape, and SOA injection current [15]. Optimal condition could be found as following. First of all, we employed RZ signal format (RZ signal format is generally faster than NRZ format in the application of optical logic gates based on XGM process [6]. This is because guard time for the carrier recovery can be guaranteed with RZ. And also note that RZ signal has the advantage of hiding static “1” hazard compared to NRZ signal). And RZ signal pulse width was set $\sim 30\%$ of the bit duration. And signal power level was determined utilizing the steady state response data of XGM process. In our whole simulations SOA parameters were also set as same with the Table 3. Based on the steady state in Fig. 7 (a), (b) and (c), we used the pump power of -10dBm (0-level) & 10dBm (1-level), together with the probe input power of -20dBm (0-level) & 0dBm (1-level) to get the wide open eyes. And then, SOA driving current was adjusted to control the carrier lifetime referring to the dynamic response of XGM process shown in Fig. 7 (d). We selected 200mA as an injection current for the operation speed of 2.5Gbps.

(a) Steady state response with 50mA

(b) Steady state response with 100mA

(c) Steady state response with 200mA

(d) Dynamic response with 200mA

Fig. 7. Steady state (a), (b), (c) and dynamic (d) response of XGM characteristics of given SOA

Output data traces (Fig. 8 (c), (d)) of the *Gray* code to BCD converter are shown in the Fig. 8 for the 2.5Gbps input signals (Fig. 8 (b)) which are injecting serially form decimal numbers “0” to “9” in Gray code expression (A higher operation speed would be possible with a shorter active region length or higher bias current [16]). Eye-diagrams are also shown in Fig. 8 (e) for the input patterns of 2^7-1 PRBS (pseudo-random bit sequence) while each input of “A”, “B”, “C” and “D” takes the different seed values for the generation of PRBS.

From the eye-diagrams for random input sequence of *Gray* code, bit pattern effects could be considered. As you can see in the Fig. 8, more clear output is observed with one-level simplification method. In contrast, severe degradation can be observed form the data in the case of the two-level simplification method approach. The measured Q factors were 7, 7, and 4 for each output of X, Y, and Z, respectively in the case of the one-level simplification method and 7, 2.8, and 2.4 in the case of the two-level simplification method.

Fig. 8. Data traces and eye diagrams of the *Gray* code to BCD converter constructed using the conventional two-level simplification method and proposed one-level simplification method

6. CONCLUSION

All-optical Gray code to BCD converter has been numerically constructed for the first time utilizing our proposed photonic-specific one-level simplification method developed from the conventional two-level simplification method used in the fields of digital electronics. We have proven that proposed one-level simplification method show better performances even reducing circuit complexity. Numerical assessment results for the *Gray* code to BCD converter show that the Q factor of above 4 can be obtained for the input signals having 20dB extinction ratio at 2.5Gbps. This research has guided readers to design all-optical combinational logic circuits so that anyone can construct any types of all-optical combinational logic circuits by presenting the detail process of designing the *Gray* code go BCD converter.

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